

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

IN RE APPLICATION OF: Koji SAKUI

SERIAL NO: New Application

GAU:

FILED: Herewith

EXAMINER:

FOR: SEMICONDUCTOR MEMORY DEVICE AND MEMORY SYSTEM

INFORMATION DISCLOSURE STATEMENT UNDER 37 CFR 1.97

COMMISSIONER FOR PATENTS
ALEXANDRIA, VIRGINIA 22313

SIR:

Applicant(s) wish to disclose the following information.

REFERENCES

- ☒ The applicant(s) wish to make of record the references listed on the attached form PTO-1449, which were submitted or cited in parent Serial No. 10/457,416, filed June 10, 2003 and Serial No. 10/078,009, filed February 20, 2002. Copies of the listed references were provided in prior application Serial No. 10/078,009, filed February 20, 2002.
- ☐ A check or credit card payment form is attached in the amount required under 37 CFR §1.17(p).

RELATED CASES

- ☐ Attached is a list of applicant's pending application(s) or issued patent(s) which may be related to the present application. A copy of the patent(s), together with a copy of the claims and drawings of the pending application(s) is attached along with PTO 1449.
- ☐ A check or credit card payment form is attached in the amount required under 37 CFR §1.17(p).

CERTIFICATION

- ☐ Each item of information contained in this information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this statement.
- ☐ No item of information contained in this information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application or, to the knowledge of the undersigned, having made reasonable inquiry, was known to any individual designated in 37 CFR §1.56(c) more than three months prior to the filing of this statement.

DEPOSIT ACCOUNT

- ☒ Please charge any additional fees for the papers being filed herewith and for which no check or credit card payment is enclosed herewith, or credit any overpayment to deposit account number 15-0030. A duplicate copy of this sheet is enclosed.

Respectfully submitted,

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Form PTO 1449 (Modified)		U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE		ATTY DOCKET NO. 248647US2S CONT		SERIAL NO. New Application	
LIST OF REFERENCES CITED BY APPLICANT				APPLICANT Koji SAKUI			
				FILING DATE Herewith		GROUP	
U.S. PATENT DOCUMENTS							
EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE IF APPROPRIATE
	AA	6,434,034	08/2002	Wallace et al.			
	AB	6,278,616	08/2001	Gelsomini et al.			
	AC	5,793,774	08/1998	Usui et al.			
	AD						
OTHER REFERENCES (Including Author, Title, Date, Pertinent Pages, etc.)							
	AE	Yoshihisa IWATA, et al. "A 35 ns CYCLE TIME 3.3 V ONLY 32 Mb NAND FLASH EEPROM," IEEE Journal of Solid-State Circuits, Vol. 30, No. 11, November 1995, pgs 1157-1164.					
	AF	Toru TANZAWA, et al. "A COMPACT ON-CHIP ECC FOR LOW COST FLASH MEMORIES," IEEE Journal of Solid-State Circuits, Vol. 32, No. 5, May 1997, pgs, 662-669.					
	AG	Hitoshi KUME, et al. "A 1.28 μ m ² CONTACTLESS MEMORY CELL TECHNOLOGY FOR A 3V-ONLY 64Mbit EEPROM," IEDM Technology Digest, December 1992, 92 pgs, 991-993.					
	AH	Hitoshi MIWA, et al. "A 140mm ² 64Mb AND FLASH MEMORY WITH A 0.4 μ m TECHNOLOGY," IEEE International Solid-State Circuits Conference, ISSCC Digest of Technical Papers, February 1996, pgs, 34-35.					
	AI	H. ONODA, et al. "A NOVEL CELL STRUCTURE SUITABLE FOR A 3.VOLT OPERATION, SECTOR ERASE FLASH MEMORY," IEDM Technology Digest, December 1992, pgs. 599-602.					
	AJ	S. KOBAYASHI, et al. "A 3.3 V-ONLY 16Mb DINOR FLASH MEMORY," ISSCC Digest of Technical Papers, February 1995, pgs, 122-123.					
	AK	F. MASUOKA, ET AL. "A NEW FLASH E ² PROM CELL USING TRIPLE POLYSILICON TECHNOLOGY: IEDM Technology Papers, February 1987, pgs. 76-77.					
	AL	Georgha SAMACHISA, et al. "A 128k FLASH EEPROM USING DOUBLE POLYSILICON TECHNOLOGY" ISSCC Digest of Technical Papers, 1987, pgs. 76-77.					
	AM	Virgil Niles KYNETT, et al. "AN IN-SYSTEM REPROGRAMMABLE 256K CMOS FLASH MEMORY," IEEE International Solid-State Circuits Conference, Digest of Technical Papers, 1998, pgs. 132-133.					
	AN	Fujio MASUOKA, et al. "NEW ULTRA HIGH DENSITY EPROM AND FLASH EEPROM WITH NAND STRUCTURE CELL," IEDM 1987, PGS, 552-555.					
	AO	Jin-ki KIM, et al. "A 120-mm ² 64 Mb NAND FLASH MEMORY ARCHIEVING 180 ns/BYTE EFFECTIVE PROGRAM SPEED," IEEE Journal of Solid-State Circuits, Vol. 32, No. 5, May 1997, pgs. 670-680.					
	AP	Masataka KATO, et al. "A 0.4 μ m ² SELF-ALIGNED CONTACTLESSMEMORY CELL TRCHNOLOGY SUITABLE FOR 256-Mbit FLASH MEMORIES, " IEDM Technology Digest, 1994, pgs. 921-923.					
		Shin-ichi KOBAYASHI, et al. "MEMORY ARRAY ARCHITECTURE AND DECORDING SCHEME FOR 3 V ONLY SECTOR ERASABLE DINOR FLASH MEMORY," IEEE Journal of Solid-State Circuits, Vol. 29, No. 4, April 1994, pgs 454-460.					
					<input type="checkbox"/> Additional References sheet(s) attached		
Examiner					Date Considered		
*Examiner: Initial if reference is considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.							